

CLAIMS

What is claimed is:

1. A method for polishing or planarizing a surface of a semiconductor device structure, comprising:
polishing a first semiconductor device structure;
analyzing a topography of an active surface of the first semiconductor device structure;
generating a force gradient based on the analyzing;
applying the force gradient to a backside of at least one second semiconductor device structure;
and
polishing the at least one second semiconductor device structure with the force gradient applied to the backside thereof.
2. The method of claim 1, wherein the polishing the first semiconductor device structure comprises CMP.
3. The method of claim 1, wherein the analyzing comprises employing a metrology technique.
4. The method of claim 1, wherein the generating comprises:
considering a height of at least one raised area on the active surface of the first semiconductor device structure; and
considering a rate of material removal from a lowermost area of the active surface of the first semiconductor device structure.
5. The method of claim 4, wherein the generating further comprises determining amounts of force to apply to at least two areas of the backside of the at least one second semiconductor device structure so as to facilitate the formation of a substantially planar active surface of the at least one second semiconductor device structure during the polishing thereof.

6. The method of claim 1, wherein the applying the force gradient comprises applying at least two different amounts of pressure to the backside.

7. The method of claim 1, wherein the polishing the at least one second semiconductor device structure comprises chemical-mechanical polishing.

8. A method for compensating for nonplanarities on an active surface of a semiconductor device structure during polishing thereof, comprising:
polishing at least one layer of a first semiconductor device structure;
analyzing a topography of an active surface of the first semiconductor device structure;
selectively applying increased amounts of pressure to at least two locations on a backside of at least one second semiconductor device relative to pressure applied to other areas of the backside, the at least two locations corresponding to raised areas on the active surface of the first semiconductor device structure following the polishing of at least one layer thereof; and
polishing the at least one second semiconductor device structure while selectively applying increased amounts of pressure.

9. The method of claim 8, wherein the selectively applying comprises applying a pressure gradient to the backside of the at least one second semiconductor device structure.

10. The method of claim 9, comprising generating the pressure gradient based at least partially on:
a height of at least one raised area on the active surface of the first semiconductor device structure following the polishing of the at least one layer of the first semiconductor device structure; and

a rate of material removal from a lowermost area on the active surface of the first semiconductor device structure following the polishing of the at least one layer of the first semiconductor device structure, the height and the rate together indicating another rate and pressure for removing material from the at least one raised area to provide a substantially planar active surface on the first semiconductor device structure.

11. The method of claim 8, wherein the polishing the at least one layer of the first semiconductor device structure comprises chemical-mechanical polishing.

12. The method of claim 8, wherein the polishing the at least one second semiconductor device structure comprises chemical-mechanical polishing.